

ANNAI J.K.K.SAMPOORANIAMMAL POLYTECHNIC COLLEGE

T.N.PALAYAM, GOBI(TK), ERODE(DT) - 638506

STAFF PROFILE

1. PERSONAL DETAILS

NAME : PRIYA V

FATHER'S NAME : VELUSAMY K

DATE OF BIRTH : 07.05.1992

SEX : FEMALE

NATIONALITY : INDIAN

BLOOD GROUP : B +VE

MARITAL STATUS : SINGLE

LANGUAGES : TAMIL, ENGLISH

EXPERIENCE : FOUR YEARS

ADDRESS : 15 VARAPPALAYAM,KOLAPPALUR(PO),
GOBI-638456, ERODE(DT)

2. EDUCATIONAL QUALIFICATIONS:

DEGREE / COURSE	INSTITUTION	UNIVERSITY	YEAR OF PASSING
M.E (VLSI Design)	VELALAR COLLEGE OF ENGINEERING AND TECHNOLOGY	ANNA UNIVERSITY, CHENNAI.	2015
B.E(ECE)	SURYA ENGINEERING COLLEGE	ANNA UNIVERSITY, CHENNAI.	2013

3. TECHNICAL SKILLS:

- Software Tools known : OrCAD, Xilinx, Tanner EDA, Mentor Graphics
- Hardware : Spartan-3E, Virtex-4, Spartan-6

4. PROJECT EXPERIENCES:

PROJECT NAME:

DURATION:

TEAM SIZE:

ENVIRONMENT:

RESPONSIBILITIES:

PROJECT DESCRIPTION:

5. AREA OF INTEREST: VLSI Design Techniques

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Digital Electronics

6. EXTRA & CO-CURRICULAR ACTIVITY:

7. PRESENTATIONS:

- Presented a paper titled **“Efficient SMS Information Alert System for Railway Passengers”** in ICC'12 held at Surya Engineering College, Erode.
- Presented a paper titled **“Artificial Human Blood Using NANO Robots”** in FESTUARY'13 held at SNS College of Technology, Coimbatore.
- Presented a paper entitled **“An Area Efficient Low Power Carry Select Adder”** in a national conference at Erode Sengunthar Engineering College, Erode.
- Presented a paper entitled **“Low Latency Successive Cancellation List Decoder Architecture for Polar Codes using 2-bit Decoding”** in the international Conference on Synergistic Evolutions in Engineering at Surya Engineering College, Erode.
- Presented a paper entitled **“Design of Polar List Decoder using 2-bit SC Decoding Algorithm”** in the National Conference on Trends in Engineering Applications and Management at Velalar College of Engineering and Technology, Thindal.

8. OTHER EXPERIENCES: NIL

